Conjugated Polymer Nanoparticles as Nano Floating Gate Electrets for High Performance Nonvolatile Organic Transistor Memory Devices

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A molecular nano-floating gate (NFG) of pentacene-based transistor memory devices is developed using conjugated polymer nanoparticles (CPN) as the discrete trapping sites embedded in an insulating polymer, poly (methacrylic acid) (PMAA). The nanoparticles of polyfluorene (PF) and poly(fluorene-alt-benzo[2,1,3]thiadiazole (PFBT) with average diameters of around 50–70 nm are used as charge-trapping sites, while hydrophilic PMAA serves as a matrix and a tunneling layer. By inserting PF nanoparticles as the floating gate, the transistor memory device reveals a controllable threshold voltage shift, indicating effectively electron-trapping by the PF CPN. The electron-storage capability can be further improved using the PFBT-based NFG since their lower unoccupied molecular orbital level is beneficial for stabilization of the trapped charges, leading a large memory window (35 V), retention time longer than 10^4 s with a high ON/OFF ratio of $>10^4$. In addition, the memory device performance using conjugated polymer nanoparticle NFG is much higher than that of the corresponding polymer blend thin films of PF/polystyrene. It suggests that the discrete polymer nanoparticles can be effectively covered by the tunneling layer, PMAA, to achieve the superior memory characteristics.

1. Introduction

Conjugated polymers, inhering in the advantages of the low cost fabrication, mechanical flexibility, and solution processability, have been widely applied in soft electronics, such as light-emitting diode, photovoltaic cells, transistors, and memories in the past decade.[1–3] Apart from conventional resistor-type memory,[4–8] transistor-type memory[9–11] is an emerging technology, which incorporates an additional charge-trapping layer beneath the semiconducting materials to realize the threshold voltage modulation, including nano-floating gate dielectrics,[12–16] ferroelectric materials,[17–19] or polymer-based electrets.[20–23] They have the advantages of nondestructive readout and multibit storage, being considered as promising candidates for next-generation nonvolatile memories. Among them, the floating gate memory which utilizes continuously conducting materials with a planer structure[24–27] or discrete metallic nanoparticles[12–14,28–30] as carrier-storage sites is one of the most studied architectures due to the controllable threshold voltages by modulating both the carrier-trapping site and tunneling layer. For example, introducing metallic nanoparticles (Au or Al),[13,14] carbon materials (such as graphene and graphene oxide),[25,26,31] inorganic or organic semiconductor (such as PCBM, Ge, and MOS_2),[32–34] into the insulating layer could effectively produce the hysteresis phenomenon to control the accumulation or depletion of mobile carriers transporting in the semiconducting channel. In addition, Kim et al. disclosed that the trapping and retention capability of the nano-floating gate memory is dependent on the morphology of differently metallic nanoparticles and electric field on the tunneling layer.[12,14] These studies showed the promising development of floating gate OFET memory devices. However, these floating gate devices require either high vacuum deposition or multiple processing steps to combine the charge-trapping sites with tunneling layer.[15,35]

Motivated by the recent progress in the metallic-based nanoparticle structure, we are interested in developing a simply solution-processed organic nano-floating electret composed of conjugated polymer nanoparticles. Conjugated polymers have attracted extensive research interest in electronic applications in terms of their advantages of low cost, mechanical flexibility, tunable electronic structures, and controllable morphology. Previously, we discovered that pendant polymers with different chain length of π-conjugated moieties, such as fluorene, thiophene, or triphenylamine, could effectively reach stable charge-trapping ability for flash- and write-once read-many type memories.[22,23,36,37] Therefore, conjugated polymers are expected to be promising materials for charge storage, because their extended π-conjugation along the molecular backbone[38] may provide sufficient capability to stabilize holes/electrons as well as aforementioned metallic material used in trapping layer.

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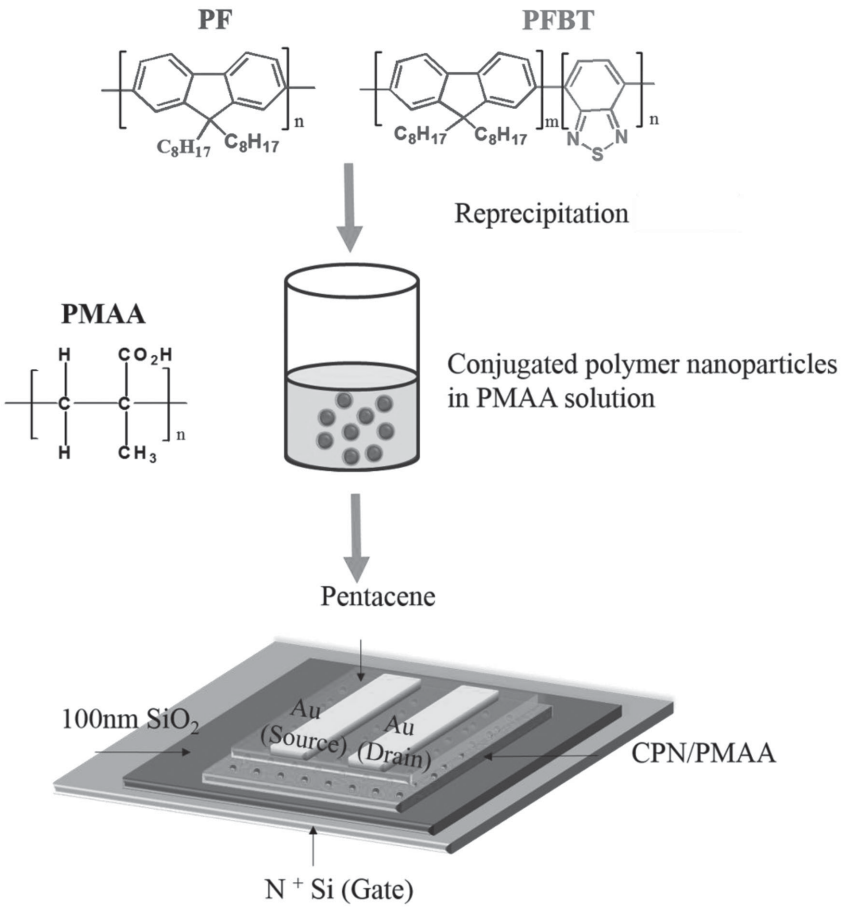

Figure 1. Schematic configuration of the proposed bottom gate/top-contact transistor memory device and chemical structures of PF and PFBT.

Furthermore, the formation of the nanoparticle morphology is supposed to be beneficial to the confinement of trapped charges.

Herein, we report a molecular nano-floating gate of pentacene based transistor memory devices using conjugated polymer nanoparticles (CPN) as the discrete trapping sites embedded in an insulating hydrophilic polymer, PMAA, as illustrated in **Figure 1**. To the best of our knowledge, this is the first report to use CPN in the transistor memory devices. Poly (9,9-dioctylfluorenyl-2,7-diyl) (PF) and poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4,8-diyl)] (PFBT) nanoparticles were prepared by the solubility-induced precipitation method by dropping a dilute solution with conjugated polymer in to a hydrophilic surroundings.[39] The effect of nanoparticle compositions (5–20 wt%) in PMAA on the memory characteristics were explored. In addition, the nanoparticles, PF, and PFBT, were used to investigate the effect of the lowest unoccupied molecular orbital (LUMO) level on the charge-transporting behavior of the memory devices. In addition, the memory performance of the blend thin films prepared from PF/polystyrene (PS) solution were used to compare those using the developed nanoparticle/polymer systems. The experimental results suggested the advantages of using the conjugated polymer nanoparticles as discrete trapping sites over the conventional polymer electret system.

2. Results and Discussion

2.1. Morphology Characterization and Photophysical Properties of CPN

CPN were prepared using the solubility-induced precipitation method. First, a hydrophobic conjugated polymer was dissolved in a good solvent, THF, and then slowly dropped into a poor solvent (water) to produce the nanoparticles. **Figure 2**a,b shows the FE-SEM images of PF nanoparticles and their particle size distribution, respectively. The image shows the PF nanoparticles are successfully prepared with average particle size of 50–70 nm, and a narrow size distribution. Note that the CPN can be well-dispersed in the solution at the concentration up to 20 wt% in water and stable suspension for at least 2 weeks. In addition, the laser confocal microscope of the PF CPN, shown in Figure 2c, exhibit a discrete blue light emission on the surface of PMAA, indicating the well-dispersion of nanoparticles in the PMAA matrix. The similar particle size and its distribution are also observed in PFBT CPN (Figure S1, Supporting Information).

The photophysical characteristics of PF homopolymer in THF solution and PF nanoparticles in water solution were investigated by optical absorption. The absorption maxima wavelengths of PF in THF solution and nanoparticle aqueous solution are observed at the wavelength of 390 ± 2 nm, attributed to the π–π^* transition of the fluorene units (**Figure 3**a, red line). However, a new peak at 435 nm is observed in the PF nanoparticle solution (Figure 3a, blue line), which is attributed to the formation of a crystalline β phase of polyfluorene.[39–41] Further evidence is shown in PL spectra of Figure 3b. The PF in THF solution possesses a vibronic structure, peaking at 424 nm (Figure 3b, red line), while the PF nanoparticles exhibit a red-shifted PL spectrum with a main peak at 439 nm. Poly(9,9-dialkylfluorene) is known to have the disordered amorphous and crystalline β phase. Compared with the disordered amorphous phase of PF, the β phase is a phase with a planar zigzag conformation to improve molecular packing, resulting in an extended conjugation length and smaller band gap.[42] The crystalline β phase could act as charge-trapping sites, and contribute to stabilize the storage charges.

The surface structure of the PF CPN/PMAA blend was investigated using AFM. The AFM images of the PF CPN/PMAA thin films spin-coated from the aqueous solutions with 0, 10, and 20 wt% CPN in PMAA, are shown in **Figure 4**a–c, respectively. The density of the nanoparticles on the surface is increased as enhancing the PF nanoparticle composition in solutions. The diameters of the 10 wt% PF nanoparticles is

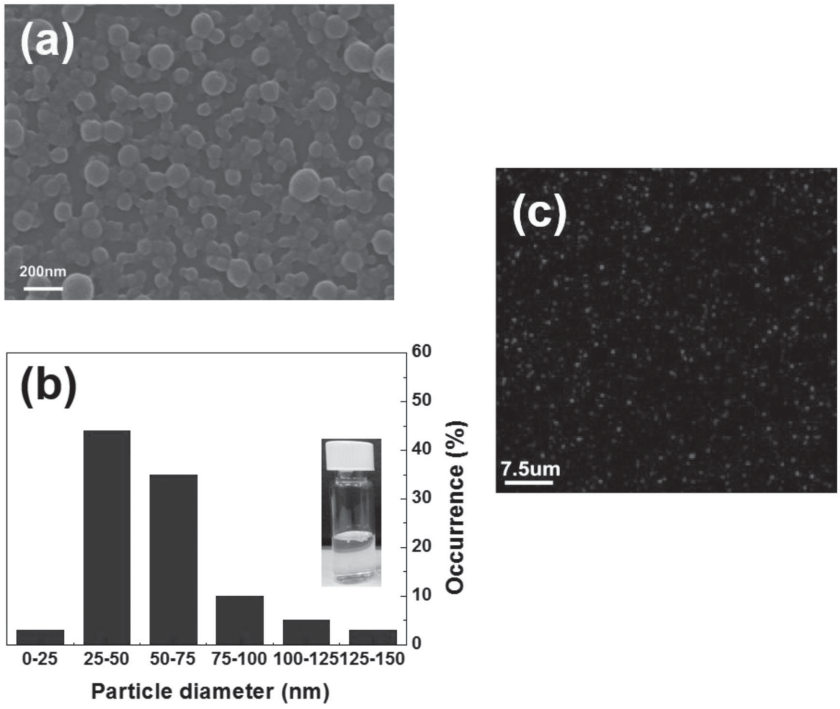

Figure 2. a) SEM images of the densely packed PF nanoparticles and b) the corresponding histograms of the nanoparticle height and c) the thin film confocal images of 10 wt% PF nanoparticles embedded in PMAA.

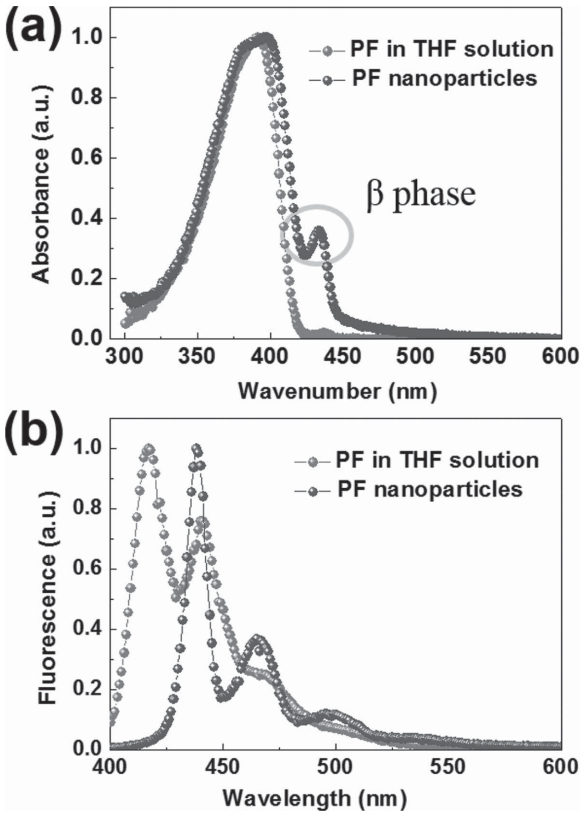

Figure 3. a) UV–vis and b) photoluminescence spectra (at the excitation wavelength of 370 nm) of PF in THF solution and PF nanoparticles.

slightly larger than that of the pristine polyfluorene nanoparticles (50 nm), probably attributed to the effective coverage by PMAA. However, large aggregated nanoparticles with diameters of 100–150 nm are observed in the 20 wt% PF CPN/PMAA film (Figure 4c), suggesting that the aggregation at a higher CPN concentration in solution.

2.2. Transistor Memory Devices Employing CPN-Based Electrets

The composite thin films with different CPN weight composition (5, 10, 15, and 20 wt%) in the PMAA matrix, denoted as PF-5, PF-10, PF-15, and PF-20, respectively, were employed as a charge-storage layer for pentacene-based transistor memory devices. As schematically shown in Figure 1a, CPN-based nano floating gate (NPG) memory devices with a bottom-gate top-contact configuration were fabricated and pentacene was used as a charge-transport layer. The spin-coated CPN/PMAA thin films with a thickness of ≈30 nm were employed as the charge-trapping layer between SiO_2 and pentacene. Note that PMAA acts as a tunneling layer due to its high dielectric constant of 8.1 for reducing the driving voltage.[26] The initial, writing, and erasing transfer curves of the CPN-based NFG devices are shown in **Figure 5**, and the related transfer characteristics are summarized in **Table 1**. Note that all scans of drain current (I_d) versus V_g are at a fixed drain voltage, V_d, of –30 V. The transfer scans applied external positive gate-source pulse (+50 V, 1 s) and negative one (–50 V, 1 s) are served as the "writing" and "erasing" processes, respectively. The devices using the CPN/PMAA electrets typically exhibit a unipolar *p*-type accumulation mode as well as the control device with PMAA as electret. The field-effect mobility (μ) extracted from the saturation region of the PMAA, PF-5, PF-10, PF-15, and PF-20 devices are 0.55, 0.45, 0.32, 0.28, and 0.27 $cm^2\ V^{-1}\ s^{-1}$, respectively (Figure S2, Supporting Information). The threshold voltage (V_{th}) and the I_{on}/I_{off} current ratio range from –4.90 to –9.56 V and 10^4 to 10^6. The mobility of the CPN/PMAA devices show a slightly decrease with the increased nanoparticle composition, probably attributed to the increased surface roughness and the decreased pentacene crystal sizes. Note that the surface roughness increases the opportunity of charge scattering. Furthermore, the pentacene on the CPN/PMAA surface with the increased CPN composition exhibited a smaller grain size (Figure 4e,f) and lower XRD intensity (Figure S3, Supporting Information), indicating the lower crystallinity of pentacene.

A control transistor memory device using the PMAA electret shows a negligible change on V_{th} even the application of the writing and erasing gate pulses (Figure 5a), similar to that reported in the literature.[26] It indicates the poor charge-trapping ability of the PMAA electret. Kim and co-workers[20]

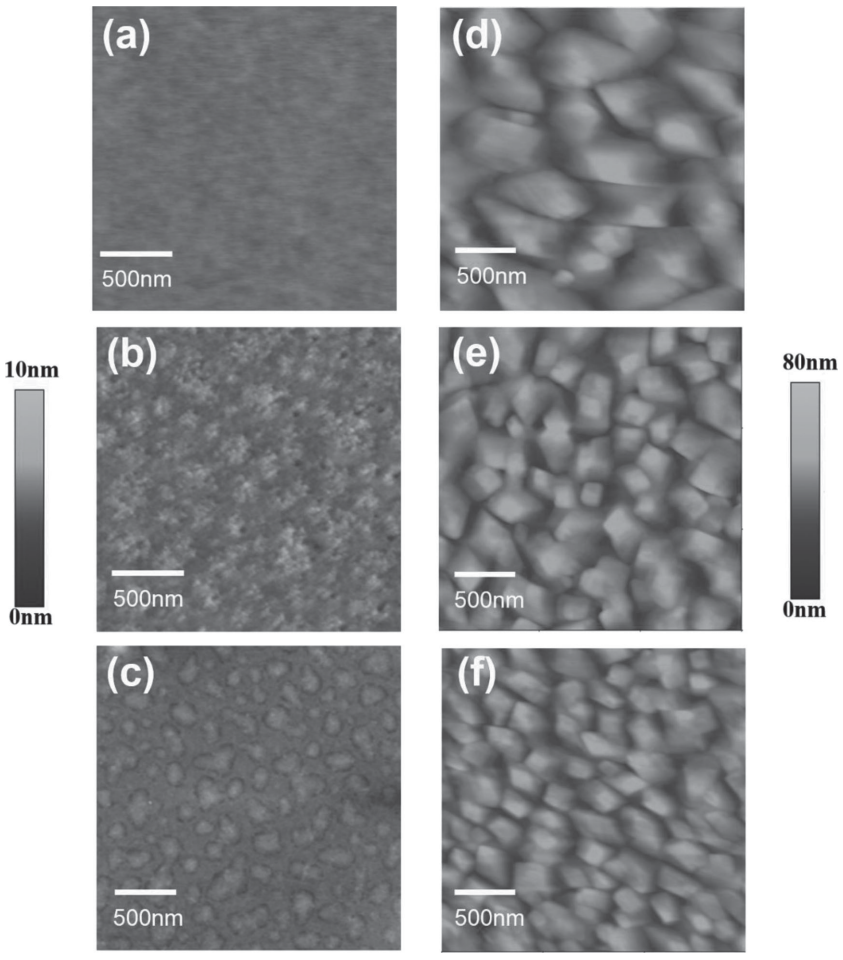

Figure 4. AFM topographies of CPN/PMAA blend films with different PF nanoparticle concentration: a) pure PMAA, b) 10 wt% PF/PMAA, c) 20 wt% PF/PMAA and the corresponding morphology after deposition of 50-nm thick pentacene on d) pure PMAA, e) 10 wt% PF/PMAA, and f) 20 wt% PF/PMAA.

demonstrated that the stability of pentacence-based transistor memory devices using a hydrophilic polymer dielectric layer was inferior to that hydrophobic or nonpolar polymers due to the conductive pathways formed from dipoles, moisture, or ions. However, they only used the hydrophilic polymer as a charge-trapping site without incorporating any semiconducting or metal particles. In our system, the memory device characteristics show an excellent stability for a few months even though using the hydrophilic PMAA. It may be attributed to the strong charge-trapping capability of the PF nanoparticles. PMAA only acts an insulating matrix and thus would not affect the long-term stability significantly. Similar results have been observed in the literature using PMAA/graphene[26] or gold nanoparticles/PVP as a charge-trapping dielectric layer.[43] The V_{th} of the CPN/PMAA devices can be easily shifted after applying the writing or erase bias, reflecting that the charges can be trapped effectively in the dispersed PF nanoparticles. The controllable V_{th} facilitates the CPN/PMAA devices to create electric bistability behavior to achieve charge storage in a single device. As shown in Figure 5b–d), the V_{th} of the programmed CPN/PMAA electrets is shifted to –3.53 (PF-5), 14.24 (PF-10), 18.40 (PF-15), and 11.22 V (PF-20), respectively. The V_{th} values can also be switched to –13.02 (PF-5), –8.44 (PF-10), –1.82 (PF-15), and –8.53 V (PF-20) after applying a reverse gate-bias. This reversible bistable switching showed this CPN/PMAA system is a potentially applicable flash-type memory. It is worth noting that higher off current and suppressed V_{th} shifts are observed in the PF-20 device. This may result from the charge percolation and current leakage via the severely aggregated particles (Figure 5d), as observed in metal-nanoparticle-based NFG devices.[12,13] Among these devices, the PF-10 device presents the largest memory window, the V_{th} difference between writing and erasing transfer curves, of 22.68 V with a charge-trapping density (Δn) of 4.81×10^{12} cm^{-2}.

The switchable threshold voltages controlled by the writing/erasing processes indicate that the electric-induced electrons in the semiconductor/electret interface can be trapped and detrapped in the PF nanoparticles. The incorporation of metallic nanoparticles and semiconducting molecules within nano-floating-gate dielectrics has been demonstrated that the trapping behavior is highly dependent on their work function and energy level.[22,43] Therefore, the alignment of energy levels for pentacene and conjugated polymer trapping moieties are used to elucidate this electron-trapping property. As shown in **Figure 6**a, the highest occupied molecular orbital (HOMO) energy levels of pentacene and PF are –5.1 and –6.0 eV, respectively; while their LUMO levels are –2.9 and –3.1 eV.[44] When applying a positive gate pulse for programming, electrons tend to accumulate at the interface between pentacene and the electret. Due to the external electrical field, the electrons on the LUMO energy level of pentacene may overcome the barrier of the PMAA matrix and are transferred to the LUMO level of PF, which could stabilize the trapped electrons due to the lower LUMO level of PF.[22,45] In order to verify this hypothesis, poly(fluorene-alt-benzo[2,1,3]thiadiazole (PFBT), a common electron-transport material with a lower LUMO level (–3.5 eV) was prepared as polymer nanoparticles and embedded in PMAA as nano-floating gate. The device containing 10 wt% PFBT CPN denoted as the PFBT-10 device, exhibits a hole mobility of 0.35 cm^2 V^{-1} s^{-1} and I_{on}/I_{off} current ratio of 10^6, which is comparable to that of PF-10 device. Compared with the PF-10 transistor memory, however, the PFBT-10 device reveals a larger V_{th} of 26.21 V during writing (Figure 6b) and maintains a V_{th} of –8.67 V after the erasing process. The memory window can be improved about 45% from 22.68 (PF-10) to 34.88 V (PFBT-10), leading to a higher trapping density up to 7.40×10^{12}. Thus, we attribute the improved charge-storage capability to the stronger electron affinity of PFBT (–3.5 eV).[24,37]

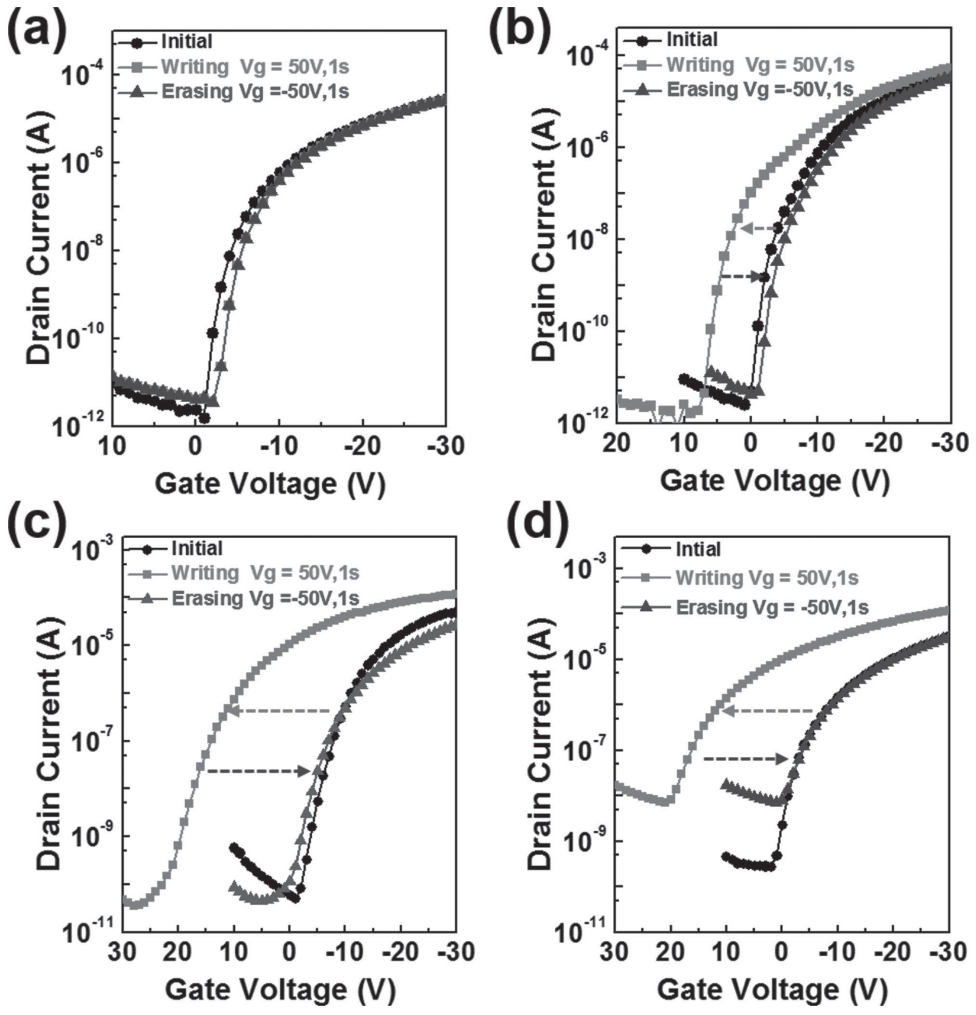

Figure 5. Transfer curves of the fabricated transistor memory devices with a) PMAA (PF-0), b) PF-5, c) PF-10, and d) PF-20. The drain current was measured at $V_{ds} = -30$ V.

2.3. Memory Devices Using PF/PS Thin Film as Charge-Storage Layer

Polymer blending approach has been employed as the polymer electret of transistor memory devices because it can simply obtain the desired properties and tunable morphology. To compare the device characteristics between polymer nanoparticle and simple polymer blend approaches, the blend film of PF and PS, as a chargeable electret, was prepared where

Table 1. The electrical and memory performance of OFET memory devices with conjugated polymer nanoparticle or blended thin film as the charge-storage layer.

	μ_{ave} [$cm^2\ V^{-1}\ s^{-1}$]	I_{ON}/I_{OFF}	$V_{th,\ ave}$ [V]	$V_{th,\ ave}$ [V]		Memory window [V]	Δn [cm^{-2}]
				Writing process	Erasing process		
PMAA(PF-0)	0.55 ± 0.02	10^6	−9.56 ± 0.8	−9.63	−9.20	–	–
PF-5	0.45 ± 0.01	10^6	−8.87 ± 0.5	−3.53	−13.02	9.47 ± 1.52	2.01×10^{12}
PF-10	0.32 ± 0.03	10^6	−4.90 ± 0.2	14.24	−8.44	22.68 ± 2.30	4.81×10^{12}
PF-15	0.28 ± 0.05	10^6	−2.53 ± 0.7	18.40	−1.82	21.22 ± 1.02	4.32×10^{12}
PF-20	0.27 ± 0.03	10^4	−5.62 ± 0.3	11.22	−8.53	19.75 ± 1.72	4.19×10^{12}
PFBT-10	0.35 ± 0.03	10^6	−5.12 ± 0.8	26.21	−8.67	34.88 ± 2.02	7.40×10^{12}
PFPS-b-10	0.72 ± 0.05	10^6	−6.74 ± 0.6	4.31	−10.20	14.51 ± 3.20	2.79×10^{12}
PFPS-b-40	0.28 ± 0.04	10^6	−6.50 ± 0.8	14.45	−9.66	20.95 ± 2.45	4.04×10^{12}

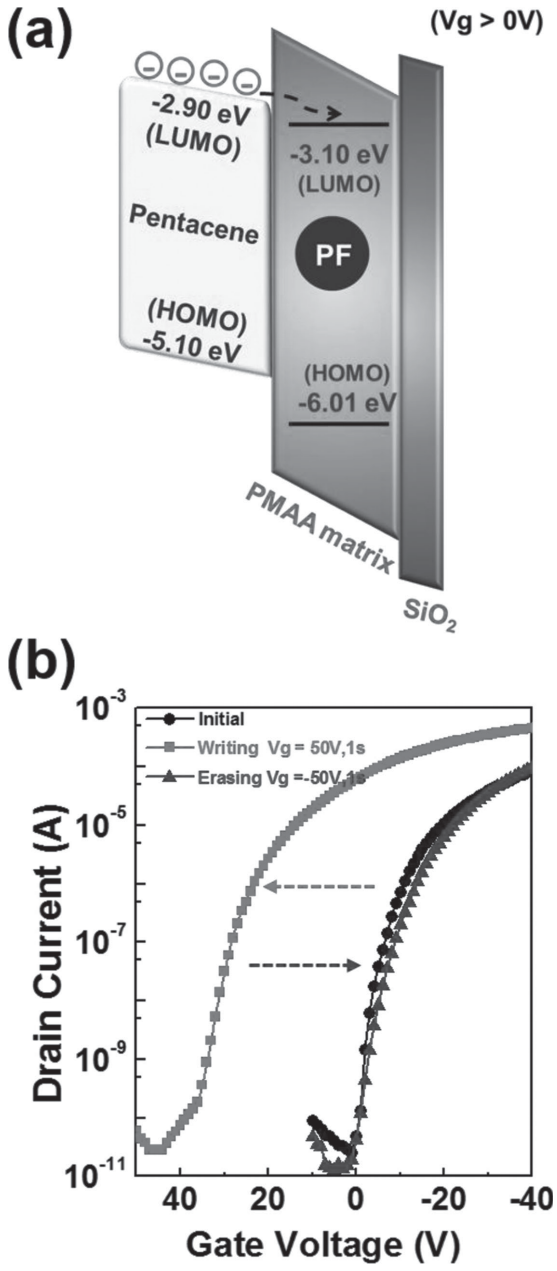

Figure 6. a) Energy diagram of pentacene and the studied conjugated polymer and the proposed charge-trapping mechanism. b) Transfer curves of the transistor memory devices using PFBT-10 electret. The drain current was measured at $V_d = -30$ V.

PS and PF are served as a tunneling layer and charge-storage sites, respectively. We chose PS as a tunneling layer, instead of PMAA, because of their close contact angles (95° for PF, and 97° for PS) and similar solubility in common organic solvents (Figure S4, Supporting Information). The blending thin films were spin-coated on 100-nm-thick SiO_2 substrates form 0.5 wt% toluene solution with different weight composition of PF (10% and 40%), which were denoted as PFPS-b-10 and PFPS-b-40. As shown in **Figure 7**a, PFPS-b-10 thin film reveals no obvious morphology and smooth surface with a low roughness of 0.32 nm. The significantly phase-separated morphologies is observed at the PFPS-b-40 film, which is composed of large spheres of 200–300 nm surrounded by the PS matrix (Figure 7b). Large phase-separated structure is also observed in other PF composition in the blend (Figure S5, Supporting Information). The strong phase separation structure is probably induced by the strong π–π stacking of polyfluorene chains.[46] The transistor memory devices based on PFPS-b-10 and PFPS-b-40 blends films were fabricated as illustrated in Figure S6 (Supporting Information), respectively. Figure 7c,d shows the characteristics of transfer curves, as listed in Table 1. The devices using PFPS-b-10 and PFPS-b-40 exhibit a high hole mobilities of 0.72 and 0.28 $cm^2 V^{-1} s^{-1}$, respectively, with a high I_{on}/I_{off} current ratio over 10^6, similar to the devices using the PF CPN/PMAA films as a polymer electret.

When applied a writing process, the initial curves displayed in Figure 7c,d are switched to positive direction from the threshold voltage of –6.74 to 4.31 and –6.50 to 14.45 V for the devices using PFPS-b-10 and PFPS-b-40, respectively. Upon the erasing operation, the V_{th} could further be recovered to the initial region with V_{th} of –10.20 V for PFPS-b-10 and –9.66 V for PFPS-b-40. The memory windows of the devices using PFPS-b-10 and PFPS-b-40 are 14.51 and 20.95 V, respectively. The OFET device incorporated with the PS electret beneath pentacene layer has no significant charge-trapping ability.[12,14,47] Therefore, the electron-trapping ability in the PFPS-b-electret OFET is definitely driven by the PF composition, consistent with the nano-floating gate system that utilizes the PF nanoparticles as trapping sites. However, for the blend system, a large amount of PF loading (>40 wt%) is required to achieve the similar memory window of the device using the PF-10 with 10 wt% conjugated polymer nanoparticles. The device using PFPS-b-10 exhibits a much smaller memory window than that using the PF-10 NFG devices with the similar PF composition. The PF/PS blend electret needs a large to reach the same memory windows as that of the 10% polymer nanoparticles could be explained as follows: The AFM image of the PF/PS blend (Figure 7b) shows that the PF aggregated domain is not completely covered by PS. Thus, pentacene could contact with PF directly and lead to the recombination between electrons and holes in the interface. Also, the absorption spectrum of the blend does not observe the β phase, which could help to stabilize the stored charge in the PF segment. Therefore, the memory window of the blend system with a similar PF loading is smaller than that of the nanoparticle system.

2.4. Retention Characteristics

The retention capability of the OFET memory devices using the PF CPN /PMAA and PF/PS blended electrets was measured after the application of +50 V (ON state) and –50 V (OFF state) gate pulses for 1 s. To compare the endurance of the bistable behavior in the different systems (PF CPN/PMAA, PFBT CPN/PMAA, and PF/PS blend), we evaluated the charge retention time in the devices using PF-10, PFBT-10, and PFPS-b-40, because these materials possessed similar particle sizes. As shown in **Figure 8**, the electrical bistability read at the zero gate-source voltage for the PF-10,

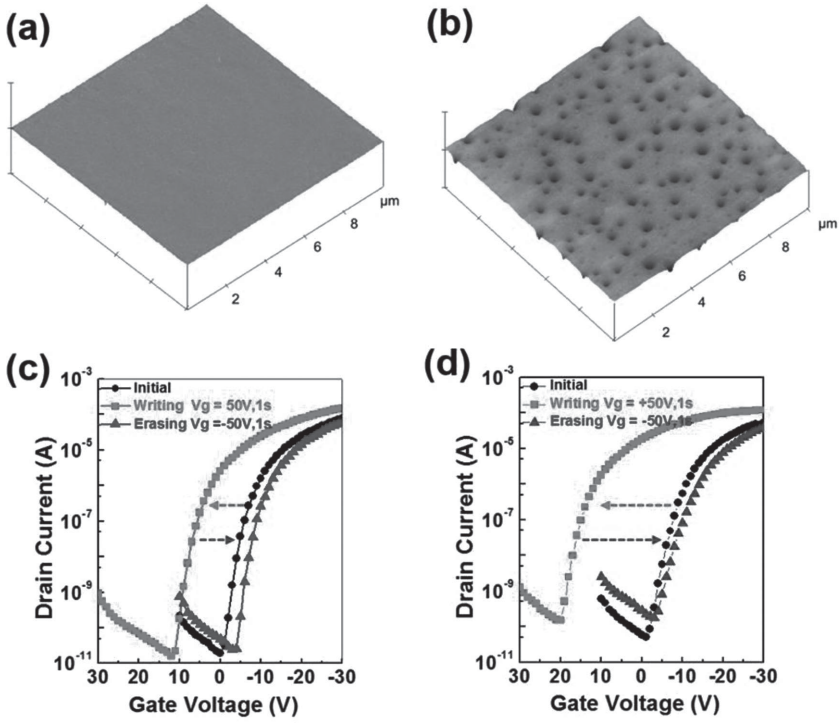

Figure 7. AFM images of PF/PS thin film with different blending ratios: a) PFPS-b-10, b) PFPS-b-40, and transfer curves of the OFET memory devices using PF/PS thin films as charge-storage layer, c) PFPS-b-10, and d) PFPS-b-40.The drain current was measured at $V_d = -30$ V.

and PFBT-10 devices could be kept at least longer than 10^4 s without any current decay, with the ON/OFF memory current ratios of 3.31×10^4 and 1.14×10^4, respectively. Although PFPS-b-40 device also could maintain the ON/OFF current state for 10^4 s, the current value of ON state gradually dissipates from 2.68×10^{-6} at beginning down to 1.70×10^{-7} at 10^4 s, where results in a smaller memory current ratios of 3.42×10^3 in comparison with the device using CPN as electrets (PF-10 and PFBT-10). The difference between the PF/PS blend film and PF CPN system is probably attributed to the lack of crystalline β phase formation in the blend, as indicated from the absorption or emission spectra (Figure S7, Supporting Information). Note that the PF/PS blend film does not use the special treatment (such as cooling to 80 K and then reheating to room temperature or exposure to certain solvent vapors.[42] and thus limit the chain packing to the crystalline β phase. In contrast, PF nanoparticles with the β phase may provide more stable energy state to store electrons than in the PF/PS blend due to the efficient energy transfer from glassy phase to the β phase, similar to those reported in the literature.[50]

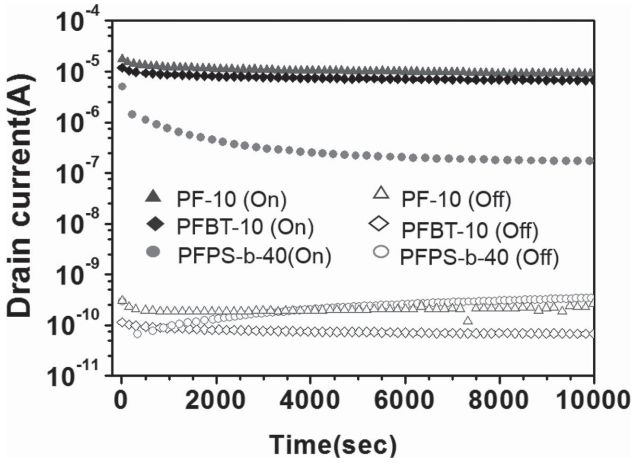

Figure 8. Retention time of the pentacene-based transistor memory device with various electrets measured at drainsource current of −30 V.

Similar situation can be observed in their corresponding writing/reading/erasing/reading (WRER) test to continuously monitor the reproducible and reversible stability for the studied devices. Note that the writing, reading and erasing are set to the gate voltages of 50, −10, and −50 V, respectively. As shown in **Figure 9**, the responding ON and OFF currents of PF-10 are maintained over 100 cycles with the conductance change of $\approx 3 \times 10^3$, showing an excellent stress endurance. It is attributed to that the insulating PMAA matrix incorporated with the separated CPN provides a high energy barrier between the CPN and semiconducting layer to effectively suppresses the occurrence of current leakage during the readout. In contrast, the ON current in WRER test of the device using the binary blending electret, PFPS-b-40, dissipates from 1.38×10^{-6} to 4.11×10^{-8} after the 100-cycle measurement, resulting in a smaller conductance change of $\approx 4 \times 10^2$ due to the incompletely phase separation. The large polyfluorene aggregate on the surface of the electret layer may contact with the semiconducting channel and lead to the depletion of trapped carriers.

As a result, the nano-floating-gate electrets prepared from conjugated nanoparticles fully covered by an insulating polymer could generate a discrete carrier-trapping structure within a tunneling layer and avoid current leakage by the simple solution process. Thus, it effectively obtains a high-performance transistor memory that has significantly trapping ability and stable retention characteristics with a high ON/OFF current ratio over 10^4 as well as the technical-leading metallic-based transistor memory.[12,14] Therefore, the proposed nano-floating-gate electret that conjugated polymer nanoparticles employed as trapping sites could achieve high performance solution-processed OFET memory applications.

3. Conclusion

In conclusion, we have developed a high performance pentacene-based transistor memory using well-separated conjugated polymer nanoparticles embedded within PMAA as the

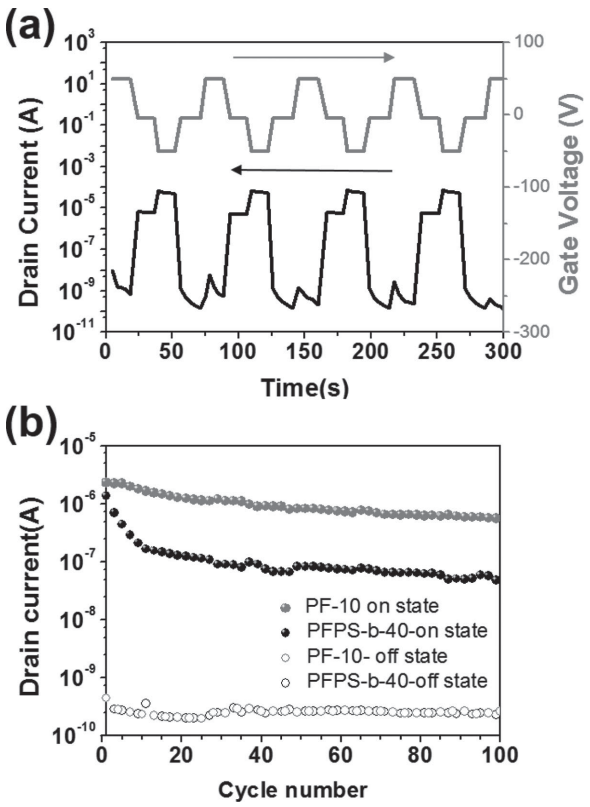

Figure 9. a) Switching behavior for PF-10 and b) record of ON and OFF current of 100 cycles for the switching behavior of PF-10 and PFPS-b-40.

nano-floating gate electret. By blending PF nanoparticles as the charge trapping segments, the transistor memories present a significantly bistable switching behavior, strongly depending on the PF CPN composition. The 10 wt% PF nanoparticle electret (PF-10) with discrete nano-floating structure is favorable to avoid current leakage occurred by nanoparticle-to-nanoparticle aggregates, resulting an obvious memory window of 22.68 V with trapping density (Δn) of 4.81×10^{12} cm^{-2}, which is much higher than the corresponding PF/PS blend film. When employed 10 wt% PFBT nanoparticle (PFBT-10) as electret to enlarge the difference of LUMO level between semiconducting layer and trapping sites, the optimized memory device exhibits an improved memory window and the largest trapping capacity up to 34.88 V and 7.40×10^{12} cm^{-2}, respectively. On the other hand, the nano-floating gate memory prepared from conjugated polymer nanoparticles is superior to the generally polymer blending system in prolonging the retention characteristics in comparison. Our proposed nano-floating conjugated nanoparticles as charge-storage sites provide a promising potential route toward the solution-processed organic transistor memories.

4. Experimental Section

Materials: Poly(9,9-dioctylfluorene) (PF, Mw = 82 000, ADS129BE), and their derivatives, Poly[(9,9-dioctylfluorenyl-2,7-diyl)-*alt*-(benzo[2,1,3] thiadiazol-4,8-diyl)] (PFBT, Mw = 157 000, ADS133YE) were purchased from American Dye Source (Quebec, Canada). Poly(metharyclic acid), Mv = 180 000 was purchased from Scientific Polymer Products (New York, USA). All of reagents or anhydrous were commercially available and used as received.

Polymer Nanoparticles Preparation: Conjugated polymer was dissolved by stirring overnight in THF under inert atmosphere. The solution was then filtered through a 0.22 μm pore size PTFE membrane filter and further diluted to a concentration of 400 ppm. A 0.2 mL quantity of the polymer/THF solution was added quickly to 8 mL of deionized water under sonication. The suspension was filtered with a 0.22 μm PTFE membrane filter, and the THF was removed by partial evaporation under vacuum. This reprecipitation process was many times to increase the nanoparticle concentration. The resulting nanoparticle dispersions were clear, with colors similar to those of the polymers in THF solution.

Transistor Memory Device Fabrication: The schematic configuration of the fabricated pentacene based transistor memory devices using conjugated polymer nanoparticle/PMAA composites is shown in Figure 1a. The highly doped Si wafer covered by a thermally grown 100-nm-thick silicon dioxide (SiO_2) was used as bottom gate substrate. The substrate was rinsed with toluene, acetone, and isopropyl alcohol and dried with a steam of nitrogen. The SiO_2 surface was treat with plasma 15 min and covered with PMAA/CPN, which was spin-coated from a 5 mg mL^{-1} water solution (700 rpm, 120 s) and baked at 50 °C on a hot plate for 60 min to remove the residual solvent. For the blend system, the PF/PS were dissolved in toluene at total concentration of 0.5 wt% by stirring overnight and then spin-coated (1600 rpm, 60 s) onto the SiO_2 layer. The thickness of the prepared thin film was estimated to be 30–40 nm. The pentacene was thermally deposited with a deposition rate of 0.3 nm s^{-1} at 25 °C under vacuum (10^{-7} torr) to form the 50 nm thick film. Source and drain gold electrodes (80 nm) were thermally evaporated through a shadow mask. The channel length (L) and width (W) of the devices were 50 and 1000 μm, respectively.

Characterization: The thickness of polymer film was measured with Microfigure Measuring Instrument (Surfcorder ET3000, Kosaka Laboratory Ltd.) The morphology of nanoparticles was performed through field emission scanning electron microscope (FE-SEM, JEOL JSM-6330F). SEM samples were sputtered with platinum prior to the images characterization and analysis was operated at accelerating of 10 kV. The morphology of polymer thin film surface were obtained with a Nanoscope 3D Controller atomic force micrographs (AFM, Digital Instruments) operated in the tapping mode at room temperature, and Fluorescence optical microscope images were taken using Two Photon Laser Confocal Microscope (Leica LCS SP5). The electrical characteristics of the fabricated transistor memory devices were measured using a Keithley 4200 semiconductor parametric analyzer. The field-effect mobility μ_{FET} (cm^2 V^{-1} s^{-1}), on/off ratios (I_{on}/I_{off}), and threshold voltages (V_{th}) of these fabricated devices were obtained using Equation (1) in the saturation regime

$$I_{ds} = \frac{WC_{tot}\mu}{2L}\left(V_g - V_{th}\right)^2 \quad (1)$$

where I_d is the drain current, V_g is the gate voltage, V_{th} is the threshold voltage, μ is the hole mobility, W is the channel width, L is the channel length, and C_{tot} is the capacitance per unit area of total dielectric layer, respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] M. T. Bernius, M. Inbasekaran, J. O'Brien, W. Wu, *Adv. Mater.* **2000**, *12*, 1737.
[2] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dotz, M. Kastler, A. Facchetti, *Nature* **2009**, *457*, 679.
[3] G. Li, V. Shrotriya, J. Huang, Y. Yao, T. Moriarty, K. Emery, Y. Yang, *Nat. Mater.* **2005**, *4*, 864.
[4] J. Ouyang, C.-W. Chu, C. R. Szmanda, L. Ma, Y. Yang, *Nat. Mater.* **2004**, *3*, 918.
[5] T. Kurosawa, T. Higashihara, M. Ueda, *Polym. Chem.* **2013**, *4*, 16.
[6] Q.-D. Ling, D.-J. Liaw, C. Zhu, D. S.-H. Chan, E.-T. Kang, K.-G. Neoh, *Prog. Polym. Sci.* **2008**, *33*, 917.
[7] C.-L. Liu, W.-C. Chen, *Polym. Chem.* **2011**, *2*, 2169.
[8] W.-P. Lin, S.-J. Liu, T. Gong, Q. Zhao, W. Huang, *Adv. Mater.* **2014**, *26*, 570.
[9] S.-T. Han, Y. Zhou, V. A. L. Roy, *Adv. Mater.* **2013**, *25*, 5425.
[10] P. Heremans, G. H. Gelinck, R. Müller, K.-J. Baeg, D.-Y. Kim, Y.-Y. Noh, *Chem. Mater.* **2010**, *23*, 341.
[11] J.-S. Lee, *J. Mater. Chem.* **2011**, *21*, 14097.
[12] M. Kang, K. J. Baeg, D. Khim, Y. Y. Noh, D. Y. Kim, *Adv. Funct. Mater.* **2013**, *23*, 3503.
[13] Q. Wei, Y. Lin, E. R. Anderson, A. L. Briseno, S. P. Gido, J. J. Watkins, *ACS Nano* **2012**, *6*, 1188.
[14] K.-J. Baeg, Y.-Y. Noh, H. Sirringhaus, D.-Y. Kim, *Adv. Funct. Mater.* **2010**, *20*, 224.
[15] S.-J. Kim, Y.-S. Park, S.-H. Lyu, J.-S. Lee, *Appl. Phys. Lett.* **2010**, *96*, 033302
[16] S. Nam, Y.-G. Ko, S. Gyu Hahm, S. Park, J. Seo, H. Lee, H. Kim, M. Ree, Y. Kim, *NPG Asia Mater.* **2013**, *5*, e33.
[17] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, D. M. de Leeuw, *Nat. Mater.* **2005**, *4*, 243.
[18] R. Schroeder, L. A. Majewski, M. Grell, *Adv. Mater.* **2004**, *16*, 633.
[19] S. Das, J. Appenzeller, *Nano Lett.* **2011**, *11*, 4003.
[20] K.-J. Baeg, Y.-Y. Noh, J. Ghim, B. Lim, D.-Y. Kim, *Adv. Funct. Mater.* **2008**, *18*, 3678.
[21] T. B. Singh, N. Marjanović, G. J. Matt, N. S. Sariciftci, R. Schwödiauer, S. Bauer, *Appl. Phys. Lett.* **2004**, *85*, 5409.
[22] Y.-C. Chiu, T.-Y. Chen, C.-C. Chueh, H.-Y. Chang, K. Sugiyama, Y.-J. Sheng, A. Hirao, W.-C. Chen, *J. Mater. Chem. C* **2014**, *2*, 1436.
[23] Y.-C. Chiu, C.-L. Liu, W.-Y. Lee, Y. Chen, T. Kakuchi, W.-C. Chen, *NPG Asia Mater.* **2013**, *5*, e35.
[24] S.-T. Han, Y. Zhou, C. Wang, L. He, W. Zhang, V. A. L. Roy, *Adv. Mater.* **2013**, *25*, 872.
[25] T.-W. Kim, Y. Gao, O. Acton, H.-L. Yip, H. Ma, H. Chen, A. K.-Y. Jen, *Appl. Phys. Lett.* **2010**, *97*, 023310.
[26] Y.-H. Chou, Y.-C. Chiu, W.-C. Chen, *Chem. Commun.* **2014**, *50*, 3217.
[27] R. H. Kim, H. J. Kim, I. Bae, S. K. Hwang, D. B. Velusamy, S. M. Cho, K. Takaishi, T. Muto, D. Hashizume, M. Uchiyama, P. André, F. Mathevet, B. Heinrich, T. Aoyama, D.-E. Kim, H. Lee, J.-C. Ribierre, C. Park, *Nat. Commun.* **2014**, *5*, 3583.
[28] H.-C. Chang, C.-L. Liu, W.-C. Chen, *Appl. Mater. Interfaces* **2013**, *5*, 13180.
[29] H.-C. Chang, C.-L. Liu, W.-C. Chen, *Adv. Funct. Mater.* **2013**, *23*, 4960.
[30] W. L. Leong, N. Mathews, S. Mhaisalkar, Y. M. Lam, T. Chen, P. S. Lee, *J. Mater. Chem.* **2009**, *19*, 7354.
[31] R. Yang, C. Zhu, J. Meng, Z. Huo, M. Cheng, D. Liu, W. Yang, D. Shi, M. Liu, G. Zhang, *Sci. Rep.* **2013**, *3*, 2126.
[32] M. Kanoun, A. Souifi, T. Baron, F. Mazen, *Appl. Phys. Lett.* **2004**, *84*, 5079.
[33] B. Kang-Jun, K. Dongyoon, K. Dong-Yu, J. Soon-Won, K. Jae Bon, N. Yong-Young, *Jpn. J. Appl. Phys.* **2010**, *49*, 05EB01.
[34] M. Sup Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S. Hwan Lee, P. Kim, J. Hone, W. Jong Yoo, *Nat. Commun.* **2013**, *4*, 1624.
[35] C.-W. Tseng, Y.-T. Tao, *J. Am. Chem. Soc.* **2009**, *131*, 12441.
[36] J.-C. Hsu, W.-Y. Lee, H.-C. Wu, K. Sugiyama, A. Hirao, W.-C. Chen, *J. Mater. Chem.* **2012**, *22*, 5820.
[37] Y.-H. Chou, S. Takasugi, R. Goseki, T. Ishizone, W.-C. Chen, *Polym. Chem.* **2014**, *5*, 1063.
[38] J. Lin, W. Li, Z. Yu, M. Yi, H. Ling, L. Xie, S. Li, W. Huang, *J. Mater. Chem. C* **2014**, *2*, 3738.
[39] C. Wu, C. Szymanski, J. McNeill, *Langmuir* **2006**, *22*, 2956.
[40] C. Wu, J. McNeill, *Langmuir* **2008**, *24*, 5855.
[41] R. Zhu, J.-M. Lin, W.-Z. Wang, C. Zheng, Wei, W. Wei Huang, Y.-H. Xu, J.-B. Peng, Y. Cao, *J. Phys. Chem. B* **2008**, *112*, 1611.
[42] T. Kawamura, M. Misaki, Y. Koshiba, S. Horie, K. Kinashi, K. Ishida, Y. Ueda, *Thin Solid Films* **2011**, *519*, 2247.
[43] S.-T. Han, Y. Zhou, Z.-X. Xu, V. A. L. Roy, T. F. Hung, *J. Mater. Chem.* **2011**, *21*, 14575.
[44] S.-T. Han, Y. Zhou, Q. D. Yang, L. Zhou, L.-B. Huang, Y. Yan, C.-S. Lee, V. A. L. Roy, *ACS Nano* **2014**, *8*, 1923.
[45] H. Kajii, K. Koiwai, Y. Hirose, Y. Ohmori, *Org. Electron.* **2010**, *11*, 509.
[46] B. Cho, K. Kim, C.-L. Chen, A. M. Shen, Q. Truong, Y. Chen, *Small* **2013**, *9*, 2283.
[47] K. Zhao, G. Zhou, Q. Wang, Y. Han, L. Wang, D. Ma, *Macromol. Chem. Phys.* **2010**, *211*, 313.
[48] Y.-C. Chiu, I. Otsuka, S. Halila, R. Borsali, W.-C. Chen, *Adv. Funct. Mater.* **2014**, *24*, 4240.
[49] T.-D. Tsai, J.-W. Chang, T.-C. Wen, T.-F. Guo, *Adv. Funct. Mater.* **2013**, *23*, 4206.
[50] A. L. T. Khan, P. Sreearunothai, L. M. Herz, M. J. Banach, A. Köhler, *Phys. Rev. B* **2004**, *69*, 085201.